REMARKS

Applicant has canceled the non-elected claims 11-17 in response to the Examiner's request.

Applicant has amended the specification to correct the informalities identified by the Examiner. Applicant believes that the objections to the specification are overcome by these amendments.

Claims 1-8 and 10 have been rejected under 35 U.S.C. 102(e) as being anticipated by Pham et al. (U.S. Patent No. 6,242,306). Claim 1 has been amended to incorporate the language of Claims 7-8, and Claims 7-8 have been canceled.

Claim 1, as amended, recites "a control gate located over the dielectric layer, wherein a first portion of the control gate extends into the gap between the first and second floating gate electrodes, wherein the first portion of the control gate is separated from the channel region by the dielectric layer and the gate dielectric layer".

In contrast, Pham et al. teaches that the control gate 26 is separated from the channel region 20 only by the barrier layer 17, and not by the tunnel layer 15. (Pham et al., Figs. 2, 9 and 10). Pham et al. specifically teaches "The tunnel layer 15 exposed within the isolation openings 27 is removed by an etching process". (Pham et al., Col. 7, lines 54-56.) "The etching process stops on the silicon substrate 16 … within the isolation openings 27". (Pham et al., Col. 7, lines 63-65.) Thus, the tunnel layer 15 is removed in the gap between the polysilicon floating gates 24. (See also, Pham et al. Fig. 9.)

For the foregoing reasons, Pham et al. fails to teach "the first portion of the control gate is separated from the channel region by the dielectric layer and the gate

dielectric layer" as recited by Claim 1. For these reasons, Claim 1 is not anticipated by Pham et al.

Claims 2-6 and 10, which depend from Claim 1, are not anticipated by Pham et al. for at least the same reasons as Claim 1.

Claim 9 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Pham et al. in view of Yang et al. (U.S. Patent No. 5,973,353).

While Yang et al. has been cited to teach a control gate having metal silicide, Yang et al. fails to remedy the above described deficiencies of Pham et al., with respect to Claim 1. Claim 9, which depends from Claim 1, is therefore allowable over Pham et al. and Yang et al. for at least the same reasons as Claim 1.

Applicant has added new Claims 18-28. Support for these claims is found throughout the specification as originally filed. No new matter is added. Consideration of these claims is respectfully requested.

New Claim 18 recites "a dielectric layer located over a first sidewall and an upper surface of the first floating gate electrode and over a first sidewall and an upper surface of the second floating gate electrode". Support for the dielectric layer is provided in the specification as originally filed by element 407.

New Claim 18 further recites "a first sidewall oxide region, having a different composition than the dielectric layer, located on a second sidewall of the first floating gate electrode" and "a second sidewall oxide region, having a different composition than the dielectric layer, located on a second sidewall of the second floating gate electrode". Support for the first and second sidewall oxide regions is

provided in the specification as originally filed by elements 442A, 443A and 444A.

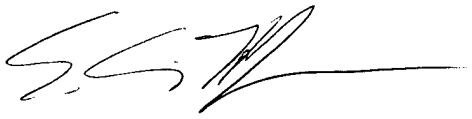
It is noted that Pham et al. does not teach or suggest "a dielectric layer", "a first sidewall oxide region" and "a second sidewall oxide region" as recited by Claim 18.

CONCLUSION

Claims 1-6, 9-10 and 18-28 are pending in the present Application. Reconsideration and allowance of these claims is respectfully requested. A document entitled "VERSION WITH MARKINGS TO SHOW CHANGES MADE" is attached.

If there are any questions, please telephone the undersigned at (925) 895-3545 to expedite prosecution of this case.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Assistant Commissioner of Patents and Trademarks, Washington, D.C., 20231, on October 14, 2002.

Oct. 14, 2002 Carrie Reddick
Date Signature

"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

SPECIFICATION

[0028] As illustrated in Fig. 4, array 100 is fabricated in a semiconductor region 401. In the described embodiment, semiconductor region 401 is a p-type well formed in a monocrystalline silicon substrate. Semiconductor region 401 has a dopant concentration of about [5e16-2e17] $5x10^{16}$-$2x10^{17}$ atoms/cm^2. In other embodiments, semiconductor region 401 can be a p-type silicon substrate. Field oxide 402 is thermally grown at the upper surface of substrate 401 using a conventional local oxidation of silicon (LOCOS) process. In the described embodiment, field oxide 402 is grown to a thickness in the range of about 4000 to 8000 Å. In the described embodiment, the field oxide is grown to a thickness of about 6000 Å. In an alternate embodiment, field oxide 402 can be replaced with a shallow trench isolation (STI) structure.

[0038] Openings 409-411 also define the diffusion bit lines of array 100. More specifically, openings 409, 410 and 411 define the locations of diffusion bit lines 131, 132 and 133, respectively. After the above-described etching steps are completed, high angle implants are performed through openings 409-411. More specifically, a P-type impurity, such as boron, is implanted through openings 409-411 at high angles with respect to the upper surface of semiconductor substrate 401, such that the dopant extends under the edges of photoresist mask 408. In accordance with one embodiment of the present invention, the high angle implants are performed by implanting P-type impurities with a dopant density in the range of [1e13 to 5e13] $1x10^{13}$ to $5x10^{13}$

ions/cm^2, and an implantation energy in the range of 40 to 100 KeV. In a particular embodiment, the high angle implants are performed with a dopant density of about [2.2e13] $2.2x10^{13}$ ions/cm^2 and an implantation energy of about 25 KeV. In one embodiment, the high angle implants are performed at angles in the range of 15 to 45 degrees from the vertical axis of Fig. 8, which extends perpendicular to the upper surface of substrate 401. In the described embodiment, the high angle implants are performed at angles approximately 25 degrees from the vertical axis of Fig. 8. The implanted boron serves to adjust the threshold voltages of NVM transistors 101-104. The implanted p-type impurities are illustrated as regions 412-414 in Fig. 8. In an alternate embodiment, the p-type impurities can be implanted along the vertical axis of Fig. 8. Note that in the described example, the pocket implant (and other process features) are less critical than in the NVM transistor 10 of Figs. 1 and 2, because a simpler process technology is being used in the present invention.

[0040] After performing the high angle implants, an N-type impurity, such as arsenic, is implanted through openings 409-411 of photoresist mask 408. In one embodiment, arsenic is implanted with a dopant density in the range of [1e15 to 1e16] $1x10^{15}$ to $1x10^{16}$ ions/cm^2 and an implantation energy in the range of 30 to 100 KeV. In a particular embodiment, arsenic is implanted with a dopant density of about [3e15] $3x10^{15}$ ions/cm^2 and an implantation energy of about 60 KeV. The implanted N-type impurities are illustrated as regions 422-424 in Fig. 9.

[0044] After the polycide etch is completed, the photoresist mask is stripped and a tungsten silicide anneal is then performed at 900°C with low oxygen flow. (This anneal adheres the tungsten silicide to the underlying polysilicon and is part of the activation of the impurities in the buried diffusion bit lines 432-434). A boron implant is then performed to prevent current leakage between diffusion bit lines at the locations between adjacent gates electrodes in the fieldless array. This boron implant is a blanket implant, with no mask protection provided on the wafer. In one embodiment, boron is implanted at a dopant density in the range of [1e12 to 6e12] $1x10^{12}$ to $6x10^{12}$ ions/cm^2 and an energy in the range of 20 to 60 KeV. In a particular embodiment, boron is implanted at a dopant density of about [3e12] $3x10^{12}$ ions/cm^2 and an energy of about 30 KeV.

[0045] Fig. 12 is a top view of NVM transistors 101-104. NVM transistors 101-102 are labeled with the reference numbers described above in Figs. 4-11. Each of NVM transistors 101-104 has a horizontal dimension of 0.72 microns (between the centers of the adjacent diffusion bit lines), and a vertical dimension of 0.5 microns. These dimensions are shown on NVM transistor 104 in Fig. 12. The area of each NVM transistor is therefore 0.36 [u^2] μ^2, with a per bit area of 0.18 [u^2] μ^2.

Page 22, on the line after "CLAIMS", add --"I Claim:"--

CLAIMS

I Claim:

1. (**Amended**) A two-bit non-volatile memory transistor comprising:

a semiconductor region having a first conductivity type;

a first source/drain region located in the semiconductor region, the first source/drain region having a second conductivity type, opposite the first conductivity type;

a second source/drain region located in the semiconductor region, the second source/drain region having the second conductivity type, wherein a channel region of the first conductivity type is located between the first and second source/drain regions;

a gate dielectric layer located over the channel region and portions of the first and second source/drain regions;

a first floating gate electrode located on the gate dielectric layer over the channel region and the first source/drain region, wherein the first floating gate electrode stores charge representative of a first data bit;

a second floating gate electrode located on the gate dielectric layer over the channel region and the second source/drain region, wherein the first and second floating gate electrodes are separated by a gap over the channel region, and wherein the second floating gate electrode stores charge representative of a second data bit;

a dielectric layer located over the first floating gate electrode and the second floating gate electrode; and

a control gate located over the dielectric layer, wherein a first portion of the control gate extends into the gap between the first and second floating gate electrodes, wherein the first portion of the control gate is separated from the channel region by the dielectric layer and the gate dielectric layer.

8. (**Canceled**)

8. (**Canceled**)

11. (**Canceled**)

12. (**Canceled**)

13. (**Canceled**)

14. (**Canceled**)

15. (**Canceled**)

16. (**Canceled**)

17. (**Canceled**)

Claims 18-28 added as new.